REMARKS

This responds to the Office Action mailed on October 28, 2004 amends claims 27-30, 33, 37, 46, and 48, cancels no claims, and adds no new claims. As a result, claims 27-49 are now pending in this application.

Claims 27-30, 33, 37, 46, and 48 have been amended to correct inadvertent typographical errors. Specifically, claims 27 and 37 have been amended to remove a space between the word "logic" and a ";", claims 28 and 29 have been amended to replace a ";" with a "." at the end of each claim, claims 30 and 46 were amended to add a "." at the end of each claim, and claims 33 and 48 were amended to delete a second "." at the end of each claim. These amendments were not made in order to overcome a rejection, and further, no prohibited new matter has been added to the application by these amendments.

Oath/Declaration (see Office Action)

The Office action stated that Exhibit A mentioned in the Declaration under 37 C.F.R. § 1.131 has not been received, and requested resubmission of Exhibit A in responding to this Office Action.

Applicant has included Exhibit A with this response, Exhibit A being the document mentioned in the Declaration under 37 C.F.R. § 1.131, the Declaration under 37 C.F.R. § 1.131 having been submitted with the response to the previous Office Action.

§*103 Rejection of the Claims*

Claims 27-31, 34-36, and 43-49

Claims 27-31, 34-36, and 43-49 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Raza (U.S. 6,640,300). Applicant does not admit that Raza is prior art and reserves the right, as provided for under 37 C.F.R. § 1.131, to "swear behind" Raza. Applicant respectfully traverses the rejection of claims 27-31, 34-36, and 43-49.

Claim 27 recites "at least one multiplexor." The Office Action on page 2 admits that "Raza does not specifically disclose the use of a multiplexer." Applicant agrees. However, the Office Action on pages 2-3 states, "Raza discloses that additional circuitry may be required to select one of the queues (see col. 4, lines 57-59). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a multiplexer in the system of Raza to control the flow of data from different inputs to a FIFO so that all the available FIFOs can be used to store data in order to improve system efficiency." Applicant disagrees with these statements. Applicant submits that "additional circuitry," as recited in Raza, does not teach or suggest "at least one multiplexor," as recited in claim 27.

Even assuming *arguendo* that "additional circuitry" teaches or suggests "at least one multiplexor," claim 27 recites,

"at least one multiplexor, including

an output coupled to the write block of one of the buffer units,

a first input coupled to the port input logic of the one buffer unit,

a second input coupled to the read block of another of the buffer units;

flow-control logic to switch the multiplexor between its first and second inputs."

Hence, Applicant submits that Raza fails to teach or suggest each of the elements of claim 27, so the Office Action fails to state a *prima facie* case of obviousness with regards to claim 27.

Further, since the cited reference does not teach or suggest "at least one multiplexer," and does not teach or suggest the additional elements of claim 27 as quoted in the paragraph above, Applicant assumes that the Examiner is taking official notice from an undisclosed source for these missing elements. Applicant objects to the taking of official notice, and pursuant to M.P.E.P. § 2144.03, Applicant traverses the assertion of official notice and requests that the Examiner cite a reference that teaches the missing elements. If the Examiner cannot cite a reference that teaches the missing elements, Applicant respectfully requests that the Examiner provide an affidavit that describes how the missing elements are present in the prior art. If the Examiner cannot cite a reference or provide an affidavit, Applicant requests withdrawal of the rejection and reconsideration and allowance of claim 27.

Claims 28-31 and 34-36 depend from claim 27. For reasons analogous to those stated above and elements in the claims, Applicant respectfully submits that the Office Action fails to state a *prima facie* case of obviousness with respect to claims 28-31 and 34-36. Therefore, Applicant requests withdrawal of the rejections and reconsideration and allowance of claims 28-31 and 34-36.

With regards to claim 43, the Office Action on page 3 states "Claims 43-49 are method claims that have substantially all the limitations of the respective apparatus claims 27-31 and 34-36. Therefore, they are subject to the same rejection." Applicant disagrees with these statements. For example, claim 43 recites,

> transmitting data from a first port input to a first buffer memory associated with the first port input and thence to a first port output;
> disabling transmitting data from a second port input to a second buffer memory associated with the second port input;
> thereafter, switching data from an output of the first buffer memory to an input of the second buffer memory, and coupling an output of the second buffer memory to the first port output." (emphasis added)

The Office Action has failed to point to any part of Raza that teaches or suggests these elements, as recited in claim 43. Therefore, Applicant submits that Raza fails to teach or suggest each of the elements of claim 43, so the Office Action fails to state a *prima facie* case of obviousness with regards to claim 43. Therefore, Applicant requests withdrawal of the rejections and reconsideration and allowance of claim 43.

Claims 44-49 depend from claim 43. For reasons analogous to those stated above and elements in the claims, Applicant respectfully submits that the Office Action fails to state a *prima facie* case of obviousness with respect to claims 44-49. Therefore, Applicant respectfully requests withdrawal of the rejections and reconsideration and allowance of claims 44-49.

Claims 32-33

Claims 32-33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Raza (U.S. 6,640,300) in view of Hendel (U.S. 6,633,976). Applicant does not admit that Hendel is prior art and reserves the right, as provided for under 37 C.F.R. § 1.131, to "swear behind" Hendel. Applicant respectfully traverses the rejection of claims 32-33.

The Office Action must provide specific, objective evidence of record for a finding of a teaching, suggestion, or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338 (Fed. Cir. 2002). Applicant submits that the statements on page 3 of the Office Action "Hendel discloses a cross-bar switch coupled between the memory and port output logic (see figure 5; col. 6, lines 44-53). Therefore, it would have been obvious to one skilled in the art to have a multi-port buffer including a cross-bar switch so that data from one input port can be routed to any of the output ports," are not supported by the record. Hendel at column 6, lines 44-55 states,

> "FIG. 5 illustrates a specific crossbar switch and associated control logic which may be implemented in one embodiment of the invention. In this embodiment, a plurality of link inputs may be coupled to input ports DIN1 through DINn, which are coupled to a plurality of input buffers 530. A crosspoint unit 520 will couple the inputs DIN1 through DINn with one or more outputs, DOUT1 though DOUTm (with one or more output buffers 540 coupled in between). The particular coupling of inputs to outputs will depend on control signals 515 transmitted from control unit 510." (emphasis added)

Applicant submits that Figure 5 of Hendel shows crosspoint 520 coupled to output buffers 540, and further, that "port output logic" does not even appear in Hendel. Hence, the statements to the contrary in the Office Action are not supported by the record. Thus, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 32-33. Therefore, Applicant requests withdrawal of the rejections and reconsideration and allowance of claim 32-33.

Even assuming *arguendo* that Raza and Hendel are not improperly combined, the Office Action still fails to state a *prima facie* case of obviousness with respect to claims 32-33. Claims 32-33 depend from claim 27, and therefore include all the elements of claim 27. For reasons analogous to those stated above and elements in the claims, Applicant respectfully submits that

Raza fails to teach or suggest all the elements of claims 32-33. Specifically, Raza fails to teach or suggest "at least one multiplexor, including an output coupled to the memory of one of the buffer units, a first input coupled to the port input logic of the one buffer unit, a second input coupled to the memory of another of the buffer units; flow-control logic to switch the multiplexor between its first and second inputs," as recited in claim 27. On pages 3-4, the Office Action admits that Hendel (with regards to claims 37, 39, and 41) does not disclose these elements, and Applicant agrees. Hence, Applicant submits that neither Raza nor Hendel, either alone or in combination, teach or suggest all the elements of claims 32-33. Thus, the Office Action fails to state a *prima facie* case of obviousness with regards to claims 32-33. Therefore, Applicant respectfully requests withdrawal of the rejections and reconsideration and allowance of claims 32-33.

Claims 37-42

Claims 37-42 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hendel (U.S. 6,633,946) in view of Raza (U.S. 6,640,300). Applicant respectfully traverses the rejection of claims 37-42.

The fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP § 2143.01.

On page 4 the Office Action states, "However, Raza discloses a multi-port buffer including memory having a write and read blocks, port input/output logics, and flow-control logic (see col. 4, lines 37-39 where Raza teaches that additional circuitry may be required to select one of the queues for reading and writing of data)." Applicant disagrees with these statements. For example, as noted above with regards to claim 27, Applicant submits that "additional circuitry" does not "implicitly disclose[s] a multiplexer" as alleged in the Office Action.

Further, Applicant submits that the statement in the Office Action on page 4, "Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to arrange the multi-port buffer as taught by Raza and to include a multiplexer in the system of Hendel in order to control and effectively use of the memory buffer," fails to meet the

standard of *In re Sang Su Lee* because it fails to point to objective evidence of record for a finding of a teaching, suggestion, or motivation to combine the reference teachings. Therefore, Applicant submits that the Office Action has failed to state a *prima facie* case of obviousness with regards to claims 37-42.

Even assuming *arguendo* that Hendel and Raza are not improperly combined, the Office Action still fails to state a *prima facie* case of obviousness with respect to claims 37-42. Claim 37 recites, "at least one multiplexor, including an output coupled to the memory of one of the buffer units, a first input coupled to the port input logic of the one buffer unit, a second input coupled to the memory of another of the buffer units; flow-control logic to switch the multiplexor between its first and second inputs." For reasons analogous to those stated above with regards to claim 27 and claims 32-33, Applicant submits that neither Raza nor Hendel, either alone or in combination, recite all the elements of claim 37. Thus, the Office Action fails to state a *prima facie* case of obviousness with regards to claim 37. Therefore, Applicant respectfully requests withdrawal of the rejections and reconsideration and allowance of claim 37.

Claims 38-42 depend from claim 37, and therefore include all the elements of claim 37. For reasons analogous to those stated above and elements in the claims, Applicant submits that the Office Action fails to state a *prima facie* case of obviousness with respect to claims 38-42. Therefore, Applicant respectfully requests withdrawal of the rejections and reconsideration and allowance of claims 38-42.

Documents Cited but Not Relied Upon for this Office Action

Applicant has reviewed the cited references that were not applied to the claims, and agrees that the claims distinguish over them in a patentable manner.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6971) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

RONALD DAMMANN ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 373-6971

Date 21 Dec 2004

By _____
J. Michael Anglin
Reg. No. 24,916

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 21 day of December, 2004.

Chris Hammond
Name

Chris Hammond
Signature

INTEL U.S. PATENT APPLICATION FILE REQUEST FORM

EXHIBIT A

COMPLETE AND RETURN FORM TO INTEL PATENT DATABASE GROUP WITHIN 2 DAYS.

Return File To: ATSK TO BE FILED BY [redacted]

Matter #: P8678 219.38327X00 Intel Grp Atty: MVS/INTEL Work Atty: ATSK

TYPE OF INTEL PATENT APPLICATION FILE

*Patent: ☐ Utility ☐ Design ☐ Reissue ☐ Reexam

☐ Continuation (C) ☐ CIP (X) ☐ Divisional (D)

Title of File: SWITCH BUFFER CONCATENATION TO SUPPORT DIFFERENT LINK DISTANCES AT FULL BANDWIDTH

INTEL DISCLOSURE AND FOREIGN FILING INFORMATION

*Disclosure number(s): 13459

*Product/Process: NGIO SWITCH, INFINIBAND SWITCH

Intel Committee: PLATFORMS Intel Group: ESG Intel Division: FCD

Foreign Filing: NO / Fast Track? NO

Countries:

Notes:

*INTEL ABSTRACT CODES (Check One or More)

__PROCESS (C1)
__N or P MOS (C1A)
__Equipment (C1B)
__CMOS (C1C)
__Contacts (C1D)
__Flash (C1E)
__GaAs and SOS (C1F)
__Circuit element (C1G)
__Isolation/Insulation (C1H)
__BICMOS (C1I)
__Analysis/Testing (C1J)
__Etching/Planarization (C1K)
__Metal (C1L)
__Poly silicon (C1M)
__Passivation (C1N)
__Masking/Resist (C1O)
__Deposition (C1P)
__Implantation (C1Q)
__DRAMs (C2)
__Sense amp (C2A)
__SRAMs (C3)
__Sense amp (C3A)
__EPROMS (C4)
__P-channel (C4A)
__N-channel (C4B)
__Flash (C4C)
__EE (C4D)
__Sense amp (C4E)
__Solid-State disk (C4F)
__Flash Card (PCMCIA) (C4G)
__Multibit Cell (C4H)
__Redundancy (C4I)
__Blocking (C4J)
__Write Automation (C4K)
__Mixcard (C4L)
__Camera (C4M)
__FWH (C4N)
__Firmware Hub (FWH) (C4O)
__Security (C4P)
__Small Block (C4Q)
__FDI (C4R)
__Interface (C4S)
__Connector (C4T)
__Cell Phone (C4U)
__Charge Pump (C4V)
__Audio (C4W)
__Microprocessor (C5)
__Embedded (C5A)
__Buses Input/Output Devices (C5B)
__Protocol/CPU Interfacing (C5C)
__Adder/Multiplier Units (C5D)
__Numeric (C5E)
__Video/Graphics (C5F)
__Cache/memory Hierarchy/Memory/Virtual Memory (C5G)
__Memory Management/Protection/Addressing (C5H)
__Instruction/Inst. Decoding/Microcoding/Sequencing/Microprogrammed Control (C5I)
__Pipeline/Parallelism (C5J)
__Clocking/Clock Generation/Clock Multiplication (C5K)
__Addressing/Addressing Modes (C5L)
__Vector Processing (C5M)
__Registers/Files/Stacks (C5N)
__Multiprocessing/Dual (C5O)
__Initialization/Testing/Debugging (C5P)
__Program/Program Control/Interrupt/Status/Faults Exceptions (C5Q)
__RISC (C5R)
__Redundancy (C5S)
✓ SYSTEMS (C6)
__Bus (C6A)
__Supercomputers (parallel multiprocessors) (C6B)
__Compilers (C6C)
__Test Equipment (ICE) (C6D)
__BIOS (C6E)
__PCMCIA (thin removable functionality cards, i.e., memory, modem, network, etc.) (C6F)
__Magnetics (bubble memories) (C7)
__Buffers (C8)
__Packaging/Mounting/Connector (C9)
__Logic (C10)
__Neural (C11)
__Miscellaneous (C12)
__General Memories (C13)
__Redundancy (C13A)
__Rambus-compatible (C13B)
__General Circuit (C14)
__Peripherals (C15)
__ROM (C16)
__Timing Clocks (C17)
__Power/Regulation (C18)
☑ Networks (C19)
__PLD (C20)
__Compression/Decompression (C21)
__Video/Graphics/Audio (C22)
__Algorithm (C22A)
__System (C22B)
__Sensor (C22C)
__Optics (C22D)
__3D (C22E)
__Display (C22F)
__Graphics Device (C22G)
__Test Equipment (C23)
__Video Teleconferencing (C24)
__Communication (C25)
__Software (C26)
__Graphics (C26A)
__Audio (C26B)
__Compiler (C26C)
__Operating System (C26D)
__Drivers (C26E)
__Other (C26F)
__IAL (C27)
__Internet/WWW Applications (C27A)
__Java Applics. (C27B)
__User Interfaces Consumer (C27C)
__Appliances Portable (C27D)
__Computing (C27E)
__Compilers (C28)
__Java Compilers (C28A)
__Java Just-in-Time (C28B)
__IA64 Compilers (C28C)
__Optimization (C28D)
__Circuits (C29)
__New Logic Family (C29A)
__Data Path (C29B)
__Chipsets (C30)
__Memory Control (C30A)
__Bridging (C30B)
__Firmware Hub (C30C)
__Design Tools (C31)
__Circuits (C31A)
__Layout (C31B)
__Logic (C31C)
__Validation/Test (C31D)
__Low Power (C31E)

*Mandatory for original patent application. File will not be opened unless mandatory information is provided.

intel
Intel Patent Database Group - EMAIL: PATENT.DATABASE.GROUP@INTEL.COM
2625 WALSH AVE. M/S SC4-203 - SANTA CLARA, CA 95051 - FAX (408) 653-7112

13469

TEL INVENTION DISCLOSU

Platforms Comm / ESG1 FCD

It is important to provide accurate and detailed information on this form. The information will be used to evaluate your invention for possible filing as a patent application. When completed and signed, please return this form to the **Legal Department at JF3-147**. If you have any questions, please call **264-0444**.

P8678
219.38327X00

1. Inventor: Dammann (Last Name) Ronald (First Name) L (Middle Initial)

Phone (408) 765-5301 M/S: SC12-105 Fax # (408) 653-5233

Citizenship: USA WWID ~~10591688~~ Contractor: YES _____ NO XXX

Inventor E-Mail Address: ronald.l.dammann@intel.com 10591699

Home Address: 3440 Ramon St#10

City Palo Alto State CA Zip 94306 Country _____

*Corporate Level Group (e.g. IABG, NCG, CEG) _____ Division _____ Subdivision _____

Supervisor* Nguyen Tran WWID 10597177 Phone (408) 765-5375 M/S: SC12-105

Inventor: McConnell (Last Name) James (First Name) A (Middle Initial)

Phone (408) 765-5397 M/S: SC12-105 Fax # (408) 653-5233

Citizenship: USA WWID 10591705 Contractor: YES _____ NO X

Inventor E-Mail Address: james.a.mcconnell@intel.com

Home Address: 850 Lewis Avenue

City Sunnyvale State CA Zip 94086 Country US

*Corporate Level Group (e.g. IABG, NCG, CEG) ESG Division FCD Subdivision _____

Supervisor* Nguyen Tran WWID 10597177 Phone (408) 765-5375 M/S: SC12-105

***If you are unsure of this information, please discuss with your manager.**

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

2. Title of Invention: Switch Buffer Concatenation to Support Different Link Distances at Full Bandwidth

3. What technology/product/process (code name) does it relate to (be specific if you can):
NGIO Switch, InfiniBand Switch

4. Include several key words to describe the technology area of the invention in addition to # 3 above: _____

5. Stage of development (i.e. % complete, simulations done, test chips if any, etc.)
Design concept that has not been implemented

6. (a) Has a description of your invention been, or will it shortly be, published outside Intel:

NO: X YES: _____ If YES, was the manuscript submitted for pre-publication approval? _____

IDENTIFY THE PUBLICATION AND THE DATE PUBLISHED: _____

(b) Has your invention been used/sold or planned to be used/sold by Intel or others?

NO: _____ YES: X DATE WAS OR WILL BE SOLD: Jan. 2000

(c) Does this invention relate to technology that is or will be covered by a SIG (special interest group)/standard/ or specification?

NO: _____ YES: X Name of SIG/Standard/Specification: NGIO/ InfiniBand

(d) If the invention is embodied in a semiconductor device, actual or anticipated date of tapeout? 12/99

(e) If the invention is software, actual or anticipated date of any beta tests outside Intel _____

7. Was the invention conceived or constructed in collaboration with anyone other than an Intel blue badge employee or in performance of a project involving entities other than Intel, e.g. government, other companies, universities or consortia? NO: X YES: _____ Name of individual or entity: _____

8. Is this invention related to any other invention disclosure that you have recently submitted? If so, please give the title and inventors: _____

PLEASE READ AND FOLLOW THE DIRECTIONS ON HOW TO WRITE A DESCRIPTION OF YOUR INVENTION

Please attach a description of the invention to this form, DATED AND SIGNED BY AT LEAST ONE PERSON WHO IS NOT A NAMED INVENTOR, and include the following information:

1. Describe in detail what the components of the invention are and how the invention works.

NGIO and InfiniBand links use flow control protocols to insure that a transmitter sending data on one end of a link does not overrun the buffer on the receiving end of the link. The receiving buffer must be large enough to hold any data that is propagating through a copper or fiber optic cable and the internal flow control processing time of the receiver and the sender. The cable data propagation time is the round trip delay of the copper or fiber optic cable connecting the sender and receiver.

NGIO uses an XON/XOFF protocol and data will be lost if cable is too long and the receive buffer is not large enough hold the data propagating through the cables.

InfiniBand uses a credit based flow control. With this type of flow control data will not be lost if the cable is too long but the link bandwidth will be limited by the cable data propagation time when long cables are used.

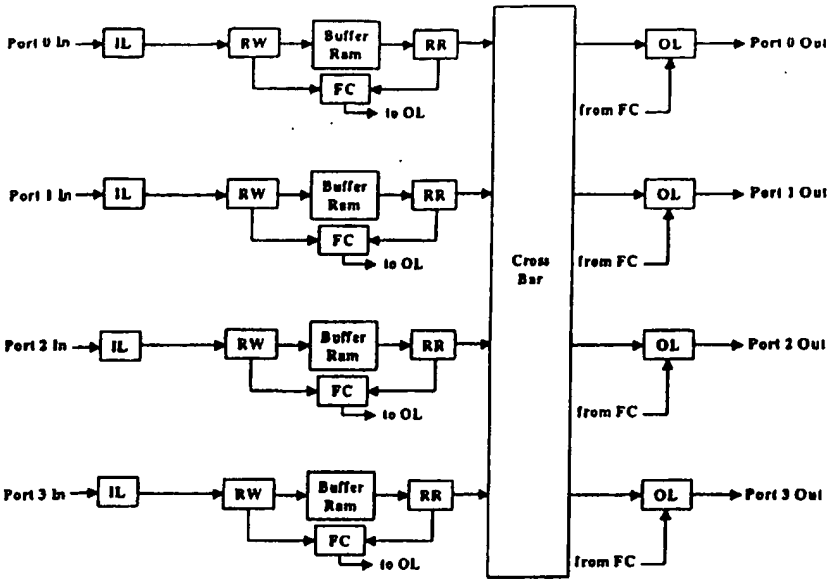
This invention proposes enhancing an NGIO/InfiniBand switch element to allow the internal buffers in each port to be combined to support longer links. An 8-port switch could be configured to support the following:

- An 8-port switch with a 1X deep buffer that supports distance 1 links.
- A 4-port switch with a 2X deep buffer that supports distance 2 links.
- A 2-port switch with a 4X deep buffer that supports distance 4 links.
- A 1-port link repeater with an 8X deep buffer that supports distance 8 links.

2. Describe advantage(s) of your invention over what is done now.

3. YOU MUST include at least one figure illustrating the invention. If the invention relates to software, include a flowchart or pseudo-code representation of the algorithm.

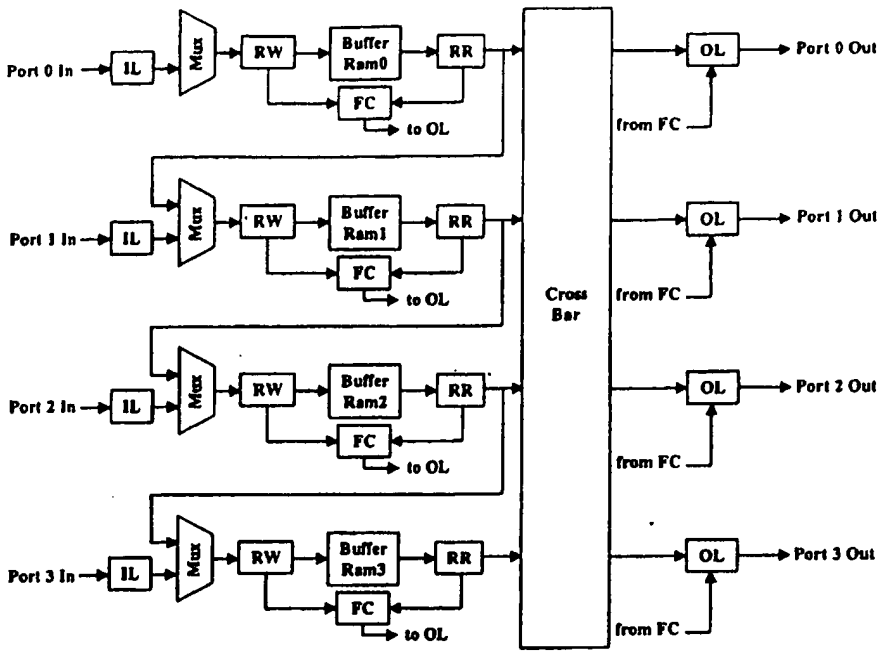
A block diagram the original 4-port NGIO switch is shown below. The actual NGIO switch has 8-ports but only 4-ports are shown to save space.



The switch has the following logic blocks:

- **IL (Input Logic).** This block receives data from the link, detects Cell/Packet boundaries and detects flow control information. This logic runs in the "input clock domain" and converts to the internal "core clock" domain. All of the other logic blocks use the "core clock"
- **RW (Ram Write)** This logic block writes packets into the Buffer Ram. I t also passes flow control information to the FC block.
- **Buffer Ram.** This buffers receive data from each port. This ram must be large enough to support the propagation delay of the external cables and determines the maximum cable length that can be supported at full link speed.
- **RR (Ram Read).** This logic block reads packets from the ram, maps the packet destination address to the correct output port, and uses the CrossBar to send the data to the correct output port. It also sends flow control information to the FC block
- **FC (Flow Control).** This logic block implements the flow control function for each port. It receives flow control information from the RW logic and sends commands to the OL logic block to start or stop sending data. It also monitors data written by the RW block and data read by the RR block to determine how much space is available in the Buffer Ram and sends flow control commands to the OL block. The OL block sends the flow control commands to the output port to pass them to the remote end and implement the flow control protocol.
- **OL (Output Logic).** This logic block sends data to the output port to send data packets or flow control commands.
- **CrossBar.** This logic block connects the RR block of each port to the OL block of each port. Any RR block can send data to any OL block. Not shown in the above block diagram is the Address Mapping Logic that maps the packet destination addresses to output ports or the Arbitration Logic that controls when RR logic from each port can send data to the OL blocks.

A block diagram of a switch supporting the port concatenation is shown below.



A multiplexor (Mux) has been added to each input port that connects the RW Block of each port to the Port's IL Block or the RR Block of another port. This allows data read from the Buffer Ram of one port to be written to the Buffer Ram of another port and increases the size of the Buffer Ram.

In normal operation the Muxes connect the IL Block to the RW Block and the switch operates as a 4-Port switch with 1X buffers.

By switching the Port 1 Mux and the Port 3 Mux the switch can be configured as a 2-Port switch with 2X buffers. In this configuration Ports 1 and 3 are disabled, Port 0 uses Buffer Ram0 and Buffer Ram1, and Port 2 uses Buffer Ram2 and Buffer Ram3.

By switching the Port 1, 2, and 3 Muxes the switch can be configured as a 1-Port link repeater with 4X buffers. In this configuration Ports 1, 2, and 3 are disabled and Port 0 uses all four Buffer Rams.

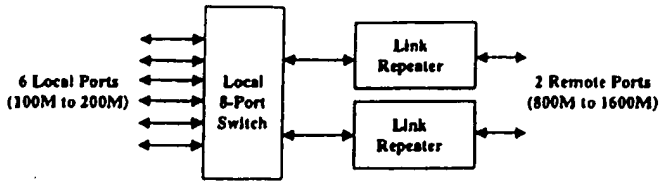
To fully implement the port concatenation the following changes are needed:

- Adding the Datapath Muxes as shown above.
- Modifying some RR and RW control signals so they work correctly in both configurations.
- Modifying the FC blocks to support the different buffer size configurations and to provide local flow control when a RR block sends data to a RW block.
- Modifying "Device Description" registers so system software can determine the port configuration of the switch.
- Modifying the IL and OL blocks to allow them to be disabled.
- Provide a way to control the port configuration. This could be:
    - External pin(s) to select the configuration of each port.
    - An external serial prom (not shown) could write a configuration register.
    - An external microprocessor (not shown) could write a configuration register.
    - An NGIO/InfiniBand command/control packet could write a configuration register.

4. Value of your invention to Intel (how will it be used?).

This would allow a single switch design to support different link distances. In most applications the switch would be configured to support short links and the maximum number of ports. With the normal NGIO/InfiniBand buffering links of 100M to 200M can be supported. By changing the configuration of a switch longer links can be supported.

One application might be to use 3 switch chips as shown in the following diagram.



The Local Switch is configured as a normal 8-Port switch and the ports are connected to other NGIO/InfiniBand devices in the same room or adjacent rooms. The two Link Repeaters are configured as 1-Port repeaters with 8 internal buffers. The Remote Ports could be connected to NGIO/InfiniBand devices on different floors or nearby buildings. (note: This would require fiber optics and the need Link Repeaters for the at the other end of the links.)

5. Explain how your invention is novel. If the technology itself is not new, explain what makes it different.

This approach allows a single switch device to be configured for different distance links without making major modifications to the basic switch design.

6. Identify the closest or most pertinent prior art that you are aware of.

7. Who is likely to want to use this invention or infringe the patent if one is obtained and how would infringement be detected?

This could be used by anybody building a NGIO/InfiniBand switch. It could also be used for 10Mb/100Mb or 1Gb Ethernet or other types of serial links with flow control protocols.

***HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM**

DATE: 12/15/99 SUPERVISOR: _____

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID

IN THE DRAWINGS

Corrected drawings are supplied herewith. Sheets 1, 2, and 3 are each identified as "REPLACEMENT SHEET". The sheets include corrections of obvious typographical errors. Specifically:

Figure 1 has been amended to replace "P_{Nri}" with "P_{N+1}" on sheet 1.

Figure 3 has been amended as follows on sheet 2:

replacement of upper most "BUFFER RAM2" in the figure with "BUFFER RAM0"

replacement of the "BUFFER RAM 2" appearing 2nd from the top in the figure with "BUFFER RAM1"

replacement of the bottom "BUFFER RAM2" in the figure with "BUFFER RAM3"

Figure 5 has been amended to replace "10′" with "100" on sheet 3.